Remarks:

Reconsideration of the application is requested.

Claims 1-6 and 16-25 are now in the application. Claims 10-15 have been cancelled. Claims 16-25 have been added. Claims 1-6 have been withdrawn from consideration.

Support for newly added claims 16-24 can be found in claims 7-15 as filed. Support for newly added claim 25 can be found in lines 22-24 on page 15 of the instant application.

In item 3 on page 2 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.83(a) for not showing the feature(s) recited in claim 10.

Enclosed are new drawings (Figs. 5a-5e) illustrating the features recited in claim 10. The appropriate amendments were also made to the specification. Support for the changes to the specification can be found in claim 10 and on page 9 of the instant application.

It is accordingly believed that the drawings and the specification meet the relevant requirements. Should the Examiner find any further objectionable items, Counsel would appreciate a telephone call during which the matter may be

resolved. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In item 5 on page 3 of the Office action, claims 10-15 have been rejected as being anticipated by *Hsu* (US 5,468,657) in view of *Sato et al.* (US 6,121,117) under 35 U.S.C. § 103 (as discussed by telephone with the Examiner on January 11, 2002).

The rejection has been noted and new claims have been entered in an effort to even more clearly define the invention of the instant application. Newly entered independent claim 16 now recites that the passivating substance X is introduced in the monocrystalline silicon layer. (This method variant is illustrated in Figs. 2a-2f).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 16 calls for, inter alia:

> fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;

introducing a ***passivating substance*** X into the ***monocrystalline silicon layer***, during or after the fabrication of the semiconductor structure; and

heat-treating the semiconductor structure with the passivating substance X for causing the passivating substance X to diffuse both to the interface and to a surface of the monocrystalline silicon layer opposite to the interface.

Hsu discloses a method for improving the electrical isolation between surface regions and underlying support regions in SIMOX buried oxide wafers by implanting nitrogen ions to approximately the same depth as oxygen ions are implanted during SIMOX processing.

The Examiner stated on page 4 of the Office action that *Hsu* discloses "introducing a passivating substance X (not labeled) ***between*** the insulation layer (59) and the monocrystalline silicon layer (3)". (emphasis added).

There is no disclosure or suggestion in either *Hsu* or *Sato et al.* to introduce a passivating substance X into a

monocrystalline silicon layer before heat-treating the semiconductor structure.

The underlying realization of the invention of the instant application is that after introducing a passivating substance X into the monocrystalline silicon layer and heat-treating the semiconductor structure with the passivating substance X and removing the screen oxide layer and subsequent growth of a gate oxide layer on the monocrystalline silicon layer, the monocrystalline silicon layer still contains sufficient passivating substance X to increase the resistance of the gate oxide layer as well with respect to damage caused by hot charge carriers. Neither *Hsu* nor *Sato et al.* suggest or disclose this underlying realization. Without considering this underlying realization, the method steps recited in claim 16 are believed not to be obvious. Therefore, the invention as recited in claim 16 of the instant application is believed not to be obvious over *Hsu* in view of *Sato et al.*.

It is accordingly believed to be clear that *Hsu* in view of *Sato et al.* do not suggest the features of claim 16. Claim 16 is, therefore, believed to be patentable over the art and since claims 17-25 are ultimately dependent on claim 16, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 16-25 are solicited.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

MARKUS NOLFF
REG. NO. 37,006

For Applicants

MN:cgm

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Version with markings to show changes made:

Replace the paragraphs on page 12, lines 1-12, with --
Figs. 3a to 3f are diagrammatic vertical sectional views of a sequence with a third design variant of the invention, in which the passivating substance X is introduced after the patterning of the silicon layer by implantation into a buried oxide layer; [and]

Figs. 4a to 4f are diagrammatic vertical sectional views of a sequence with a fourth design variant of the invention, in which the passivating substance X is introduced after the patterning of the silicon layer by implantation into the silicon layer [.], and

Figs. 5a to 5e are diagrammatic vertical sectional views of a BESOI sequence in which a passivating substance X is introduced before the joining of two silicon layer.--

Insert the following paragraph into line 24 on page 19 --
A further possibility is to introduce the passivating substance X into the SOI semiconductor structure by means of a diffusion step is illustrated in Figs. 5a -5e. A suitable fabrication method for this purpose, for SOI semiconductor

structures, is known in the art as a BESOI (Bonded Etched-back Silicon on Insulator) method. In this method, two silicon semiconductor substrates are firstly provided (Fig. 5a). A surface oxide layer is then formed on each one of the two silicon semiconductor substrates (Fig. 5b). Introducing a passivating substance X into at least one of the oxide layers before or after an oxidation step into one of the silicon semiconductor substrates (Fig. 5c). The two silicon semiconductor substrates are then joined by contacting the two oxide layers (Fig. 5d) and one of the silicon semiconductor substrates is partially removed for forming the monocrystalline silicon layer (Fig. 5e).--